Integrated Circuits Design Engineer

Job Description

We are offering an engineering/applied position in the realm of microelectronics readout integrated circuits for particle physics detectors. The role is situated within Center of Applied Physics and Advanced Detection Systems (CAPADS) at CTU in Prague. It entails conducting research and development on integrated circuits aimed at developing front-end readout chips, that are suitable for the measurement of X-rays, beta radiation and ions, primarily dedicated to the dose rate measurement and basic spectroscopy.

As an engineer/physicist in this role, your responsibilities encompass developing architectures for readout Application-Specific Integrated Circuits (ASICs). We are particularly interested in candidates with hands-on experience in full custom design, including schematic creation, layout design, simulations, physical verification, and debugging. Prior experience in the design of High-Speed Differential Drivers, Phase-Locked Loops (PLL), Control Systems, Analog-to-Digital (ADC) or Digital-to-Analog (DAC) converters would be considered advantageous.

During the upcoming year your role will be to redesign the front-end readout chip developed in 180 nm into the 65 nm technology. Alongside, you will be asked to help with modifications of an existing design in 65 nm technology using Cadence IC design tools.

Candidate Profile

Essential Skills and Experience:

- expertise in the design, simulation, and layout of CMOS integrated circuits,
- professional experience with a full-custom design flow and methodology,
- a passion for CMOS circuit design and technology, along with a willingness to understand our specific application to effectively integrate the two,
- good analytical and problem-solving skills,
- an enthusiasm for working in a small team, collaboratively crafting practical solutions in close partnership with users and external collaborators.
Desired Skills and Experience:
- Experience with Design for Manufacturing (PVT corners, reliability),
- Layout Parameter Extraction (LPE) simulations,
- Analog behavioral modeling (Verilog-A/Verilog-AMS),
- Laboratory experience in silicon bring-up and validation.

Eligibility Criteria:
- You have a professional background in Electronics Engineering (or a related field such as applied or experimental physics),
- Master's / Ph.D. degree with few years of relevant experience.

Additional Information
Contract duration: 24 months, with possible extensions.
Possible start date from: 01-March-2024.

What we offer:
- full-time,
- work in a versatile team,
- access to scientific and computing infrastructure,
- trainings and participation in international workshops and/or conferences,
- 30 days of paid leave per year,
- work in the central location of Prague, Czech republic,
- competitive salary.

About us
The CAPADS group originated at the Institute of Physics of the Czech Academy of Sciences, where we participated in the development and manufacturing of ATLAS Pixel sensors and detection modules as well as in the Medipix project. Since 2012, the group joined FNSPE CTU where it widened its scope and focus to independent development of ASIC (in CMOS 180nm and 65nm) targeting both hybrid and monolithic strip/pixel detectors. On top of this, the group handles other aspects of the DAQ chain including read-out electronics and associated software/firmware tools. Members of the team have still good presence in the high energy physics community, namely in the RD50/DRD3 collaborations, experiments from both CERN and BNL and ranging all the way to space dosimetry applications.
Group capabilities:
- analog, digital & mixed-signal ASIC design,
- experience with Cadence Virtuoso, Incisive, Calibre, Assura, PVS, Genus and other associated tools,
- Synopsis and Silvaco TCAD simulations, Geant4 and Allpix2 particle simulations,
- pre- and post-silicon verification,
- SW & FW development, PCB design, device testing,
- energy and performance calibrations, beam test evaluation,
- TID, NIEL and SEE testing using 60Co, reactor neutrons and high-energy particle beams,
- intense cooperation with local industry.

Please send your CVs to capads@fjfi.cvut.cz by 29. 2. 2024 inclusive.

Take Part! http://capads.fjfi.cvut.cz/

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Dean of FNSPE
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